# ABSTRACT OF THE DISCLOSURE

A clocked cascadable power regulator including synchronization logic and PWM control logic. The synchronization logic receives a clock signal and asserts a digital output signal synchronized with the clock signal in response to assertion of a digital input signal. The PWM control logic controls a PWM cycle in response to the digital input signal and in response to an output control condition. The regulator may be used alone or cascaded with other similar regulators for implementing a multiphase power converter with multiple channels. The clocked cascadable regulator uses digital signals to communicate between channels. Digital signals are not prone to the same kind of signal degradation or noise susceptibility as analog signals. In the cascaded configuration, there is one clock common to all channels which ensures that the phase separation between the channels is symmetrical to within the jitter tolerance of the common clock.